

Lennon

SMSC micom

CPU : INTEL PINEVIEW-M
Chip Set : INTEL TIGERPOINT-M
Remarks : DC/SC, DDR3, LV

Model Name : PINE TRAIL-M
PCB Part No : BA41-01494A(GCE)
BA41-01495A(NANYA)
BA41-01496A(HANNSTAR)
BA41-01497A(GBM)
Dev. Step : PR
Revision : 0.95
T.R. Date : 2010.12.29

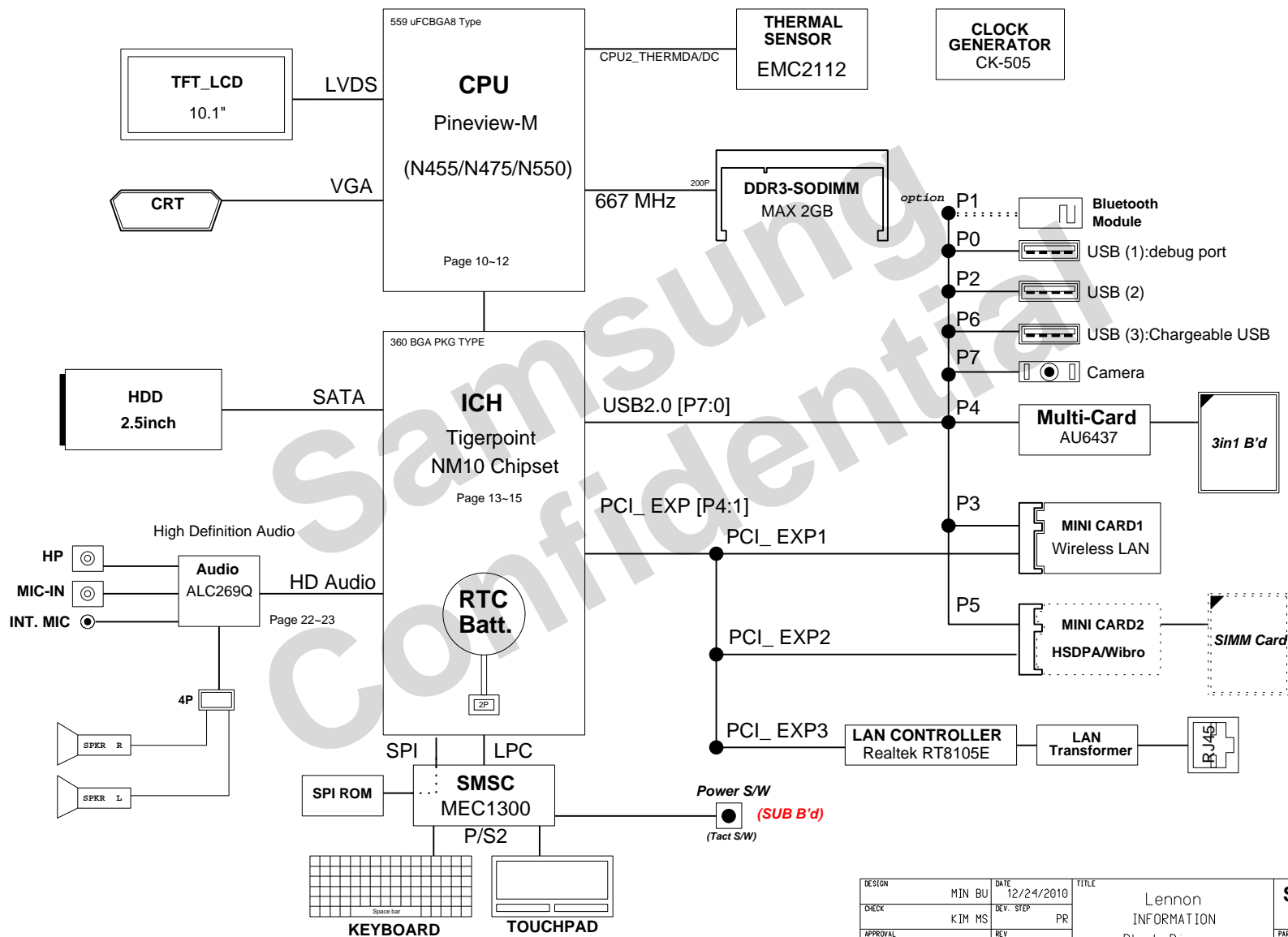
DRAW	CHECK	APPROVAL

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DESIGN	MIN BU	DATE	12/24/2010	TITLE Lennon MAIN COVER	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR		
APPROVAL	LEE HS	REV	0.95		
MODULE CODE				LAST EDIT	PART NO.
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OPERATION BLOCK DIAGRAM

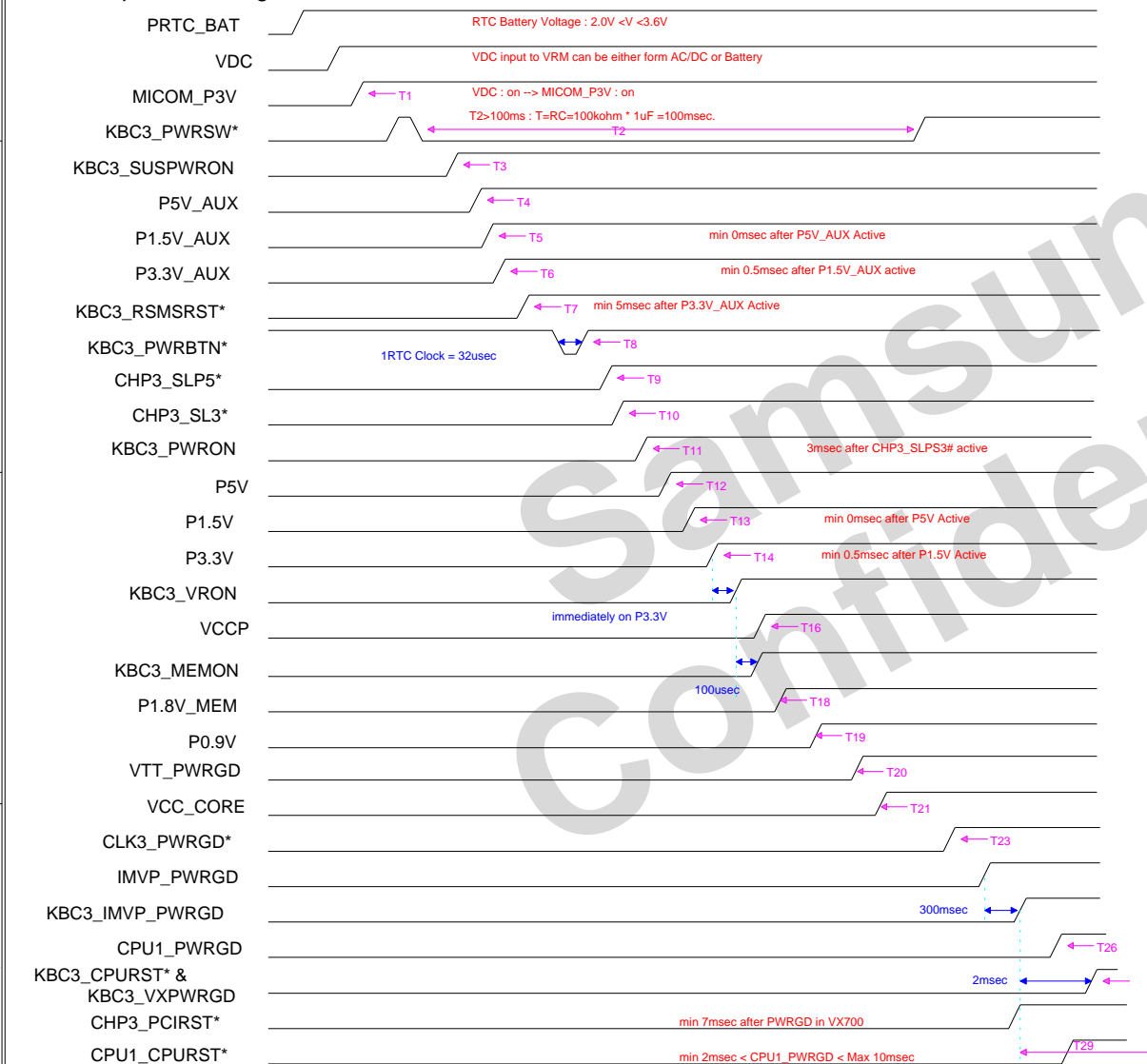


DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR	INFORMATION	Block Diagram	
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	2 OF 43	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Power Sequence Timing



PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB Hub to PCI	AD29(internal)	Programmable	
LPC Bridge/IDE/AC97/SMBUS	AD30(internal)		
Internal MAC	AD31(internal)		
	AD24(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
TigerPoint	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	
CPU Thermal Sensor	0111 101X	7Ah	Thermal Sensor

USB PORT Assign

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCI_0	0	UHCI_2	4
UHCI_1	1	UHCI_3	5
	2		6
	3		7

USB Port (Debug port)

Touchscreen Pannel

USB Port (For WLAN/WWAN)

Mini Card (For WLAN/WWAN)

CardBus Cont.

Bluetooth Module

USB Port (Chargeable)

CAMERA

PCI Express Assign

Port Number	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	Mini Card 2 (HSDPA/Wibro)
3	LOM

Voltage Rails

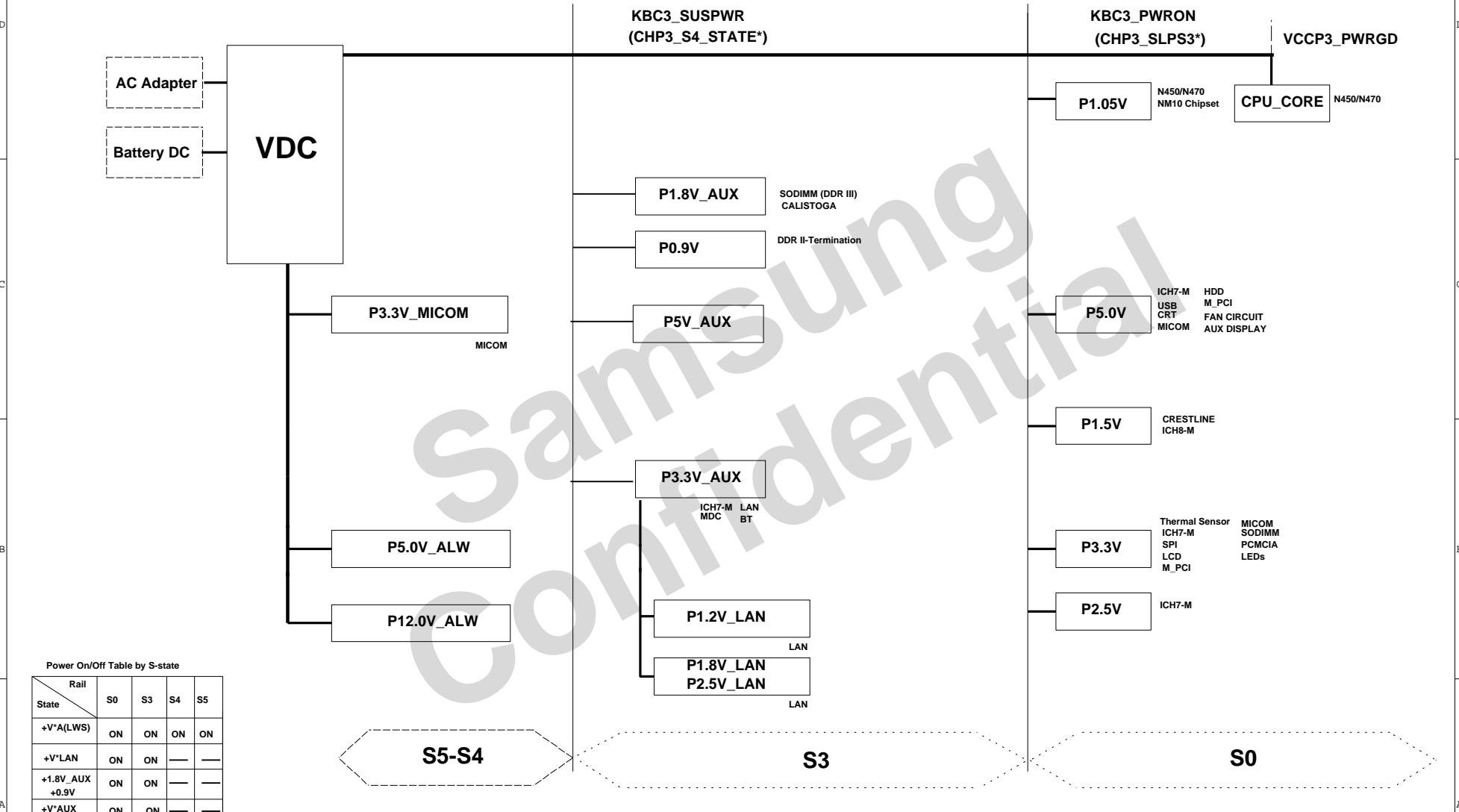
Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Callistoga & ICH7-M
P3.3V_MICOM	3.3V always power rail(for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU

DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG
CHECK	KIM MS	DEV. STEP	PR	INFORMATION	Board Information	ELECTRONICS
APPROVAL	LEE HS	REV	0.95			PART NO. BA41-01494A
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	3	OF 43

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POWER DIAGRAM

Rev 0.1



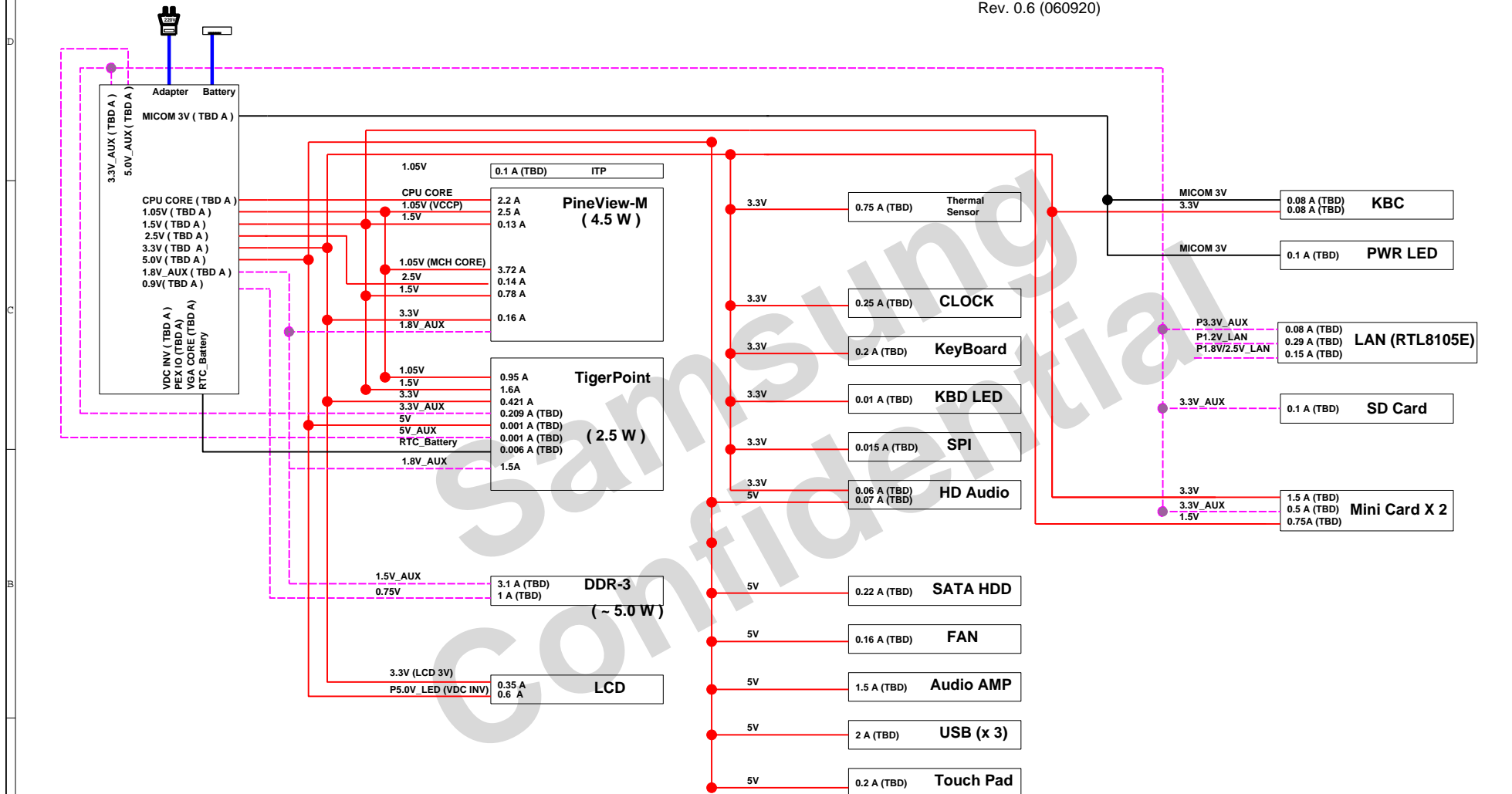
Power On/Off Table by S-state

Rail	S0	S3	S4	S5
State				
+V*A(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	—	—
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR	INFORMATION	Power Diagram	
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MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	4 OF 43	

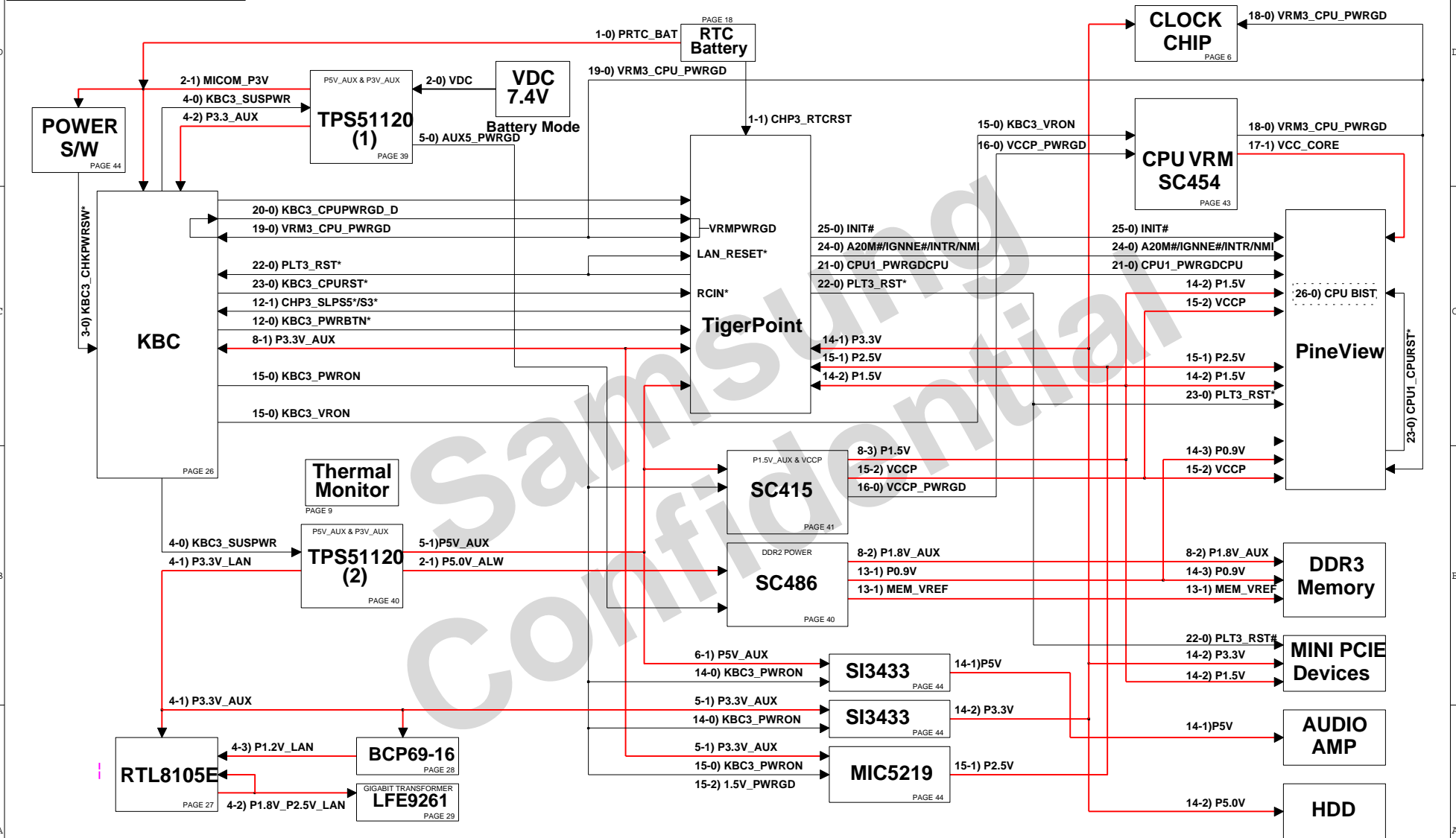
POWER RAILS ANALYSIS

Rev. 0.6 (060920)



DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS PART NO. BA41-01494A
CHECK	KIM MS	DEV. STEP	PR	INFORMATION	Power Rail Analysis	
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	5 OF 43	

POWER SEQUENCE BLOCK DIAGRAM

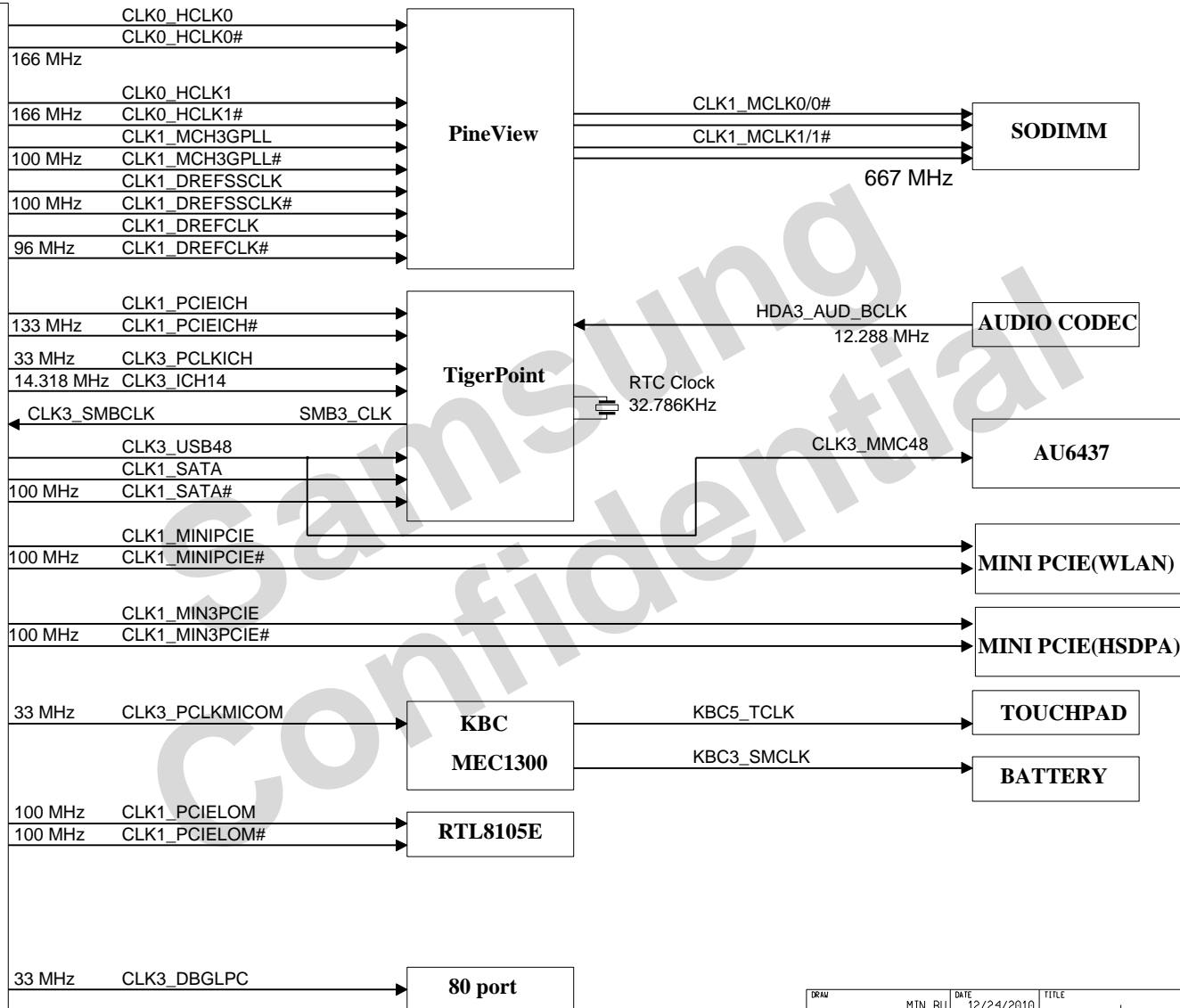


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APPROVAL	LEE HS	REV	0.95	Power Sequence Block		PART NO. BA41-01494A
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	6	OF 43

CLOCK DISTRIBUTION

1205-002574

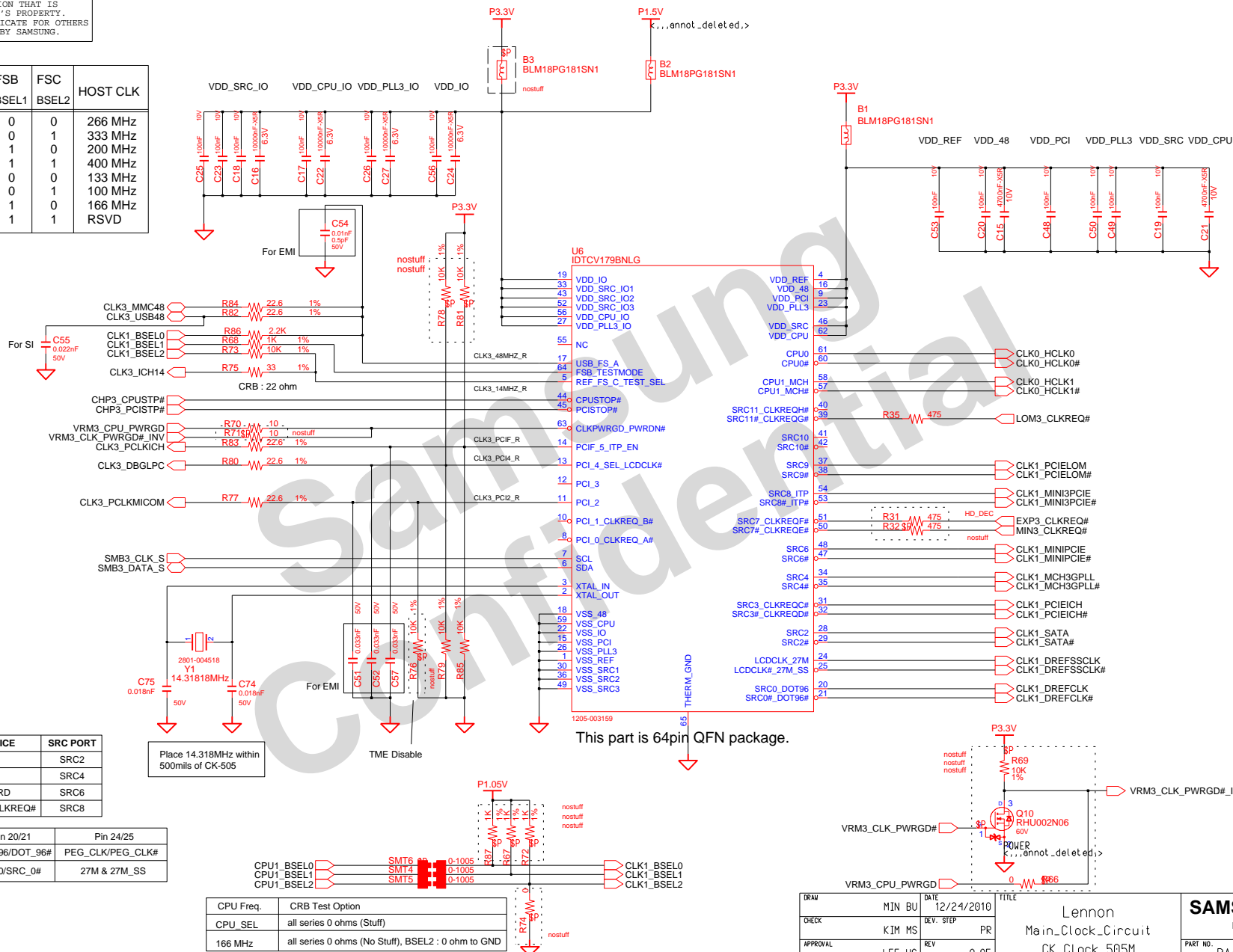
CLOCK GENERATOR
CK-505M
IDTCV179BNLG



DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG
CHECK	KIM MS	DEV. STEP	PR	INFORMATION		ELECTRONICS
APPROVAL	LEE HS	REV	0.95	Clock Distribution	PART NO.	BA41-01494A
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	7	OF 43

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FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

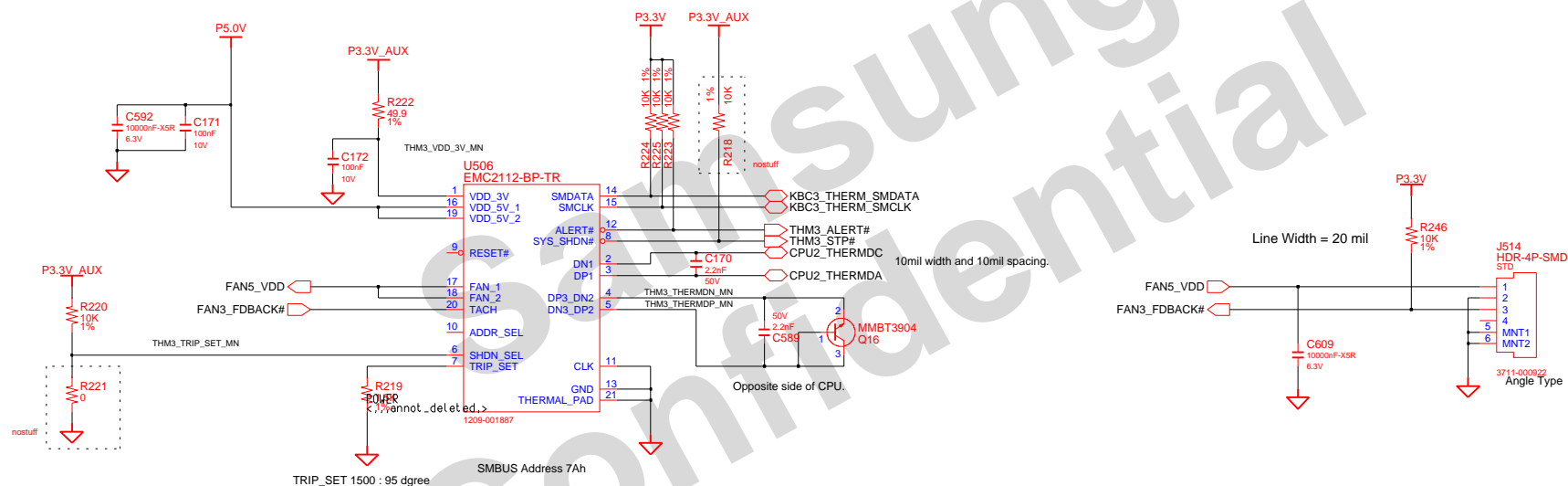
CPU Freq.	CRB Test Option
CPU_SEL	all series 0 ohms (Stuff)
166 MHz	all series 0 ohms (No Stuff), BSEL2 : 0 ohm to GND

DRAM	MIN BU	DATE	12/24/2010	TITLE	SAMSUNG ELECTRONICS	PART NO. BA41-01494A
CHECK	KIM MS	DEV. STEP	PR	Lennon Main_Clock_Circuit		
APPROVAL	LEE HS	REV	0.95	CK_Clock_505M		
MODULE CODE	undef ined	LAST EDIT	December 29, 2010 21:04:12 PM	PAGE 8 OF 43		

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THERMAL SENSOR & FAN CONTROL



DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS PART NO. BA41-01494A
CHECK	KIM MS	DEV. STEP	PR	Thermal Sensor EMC2112		
APPROVAL	LEE HS	REV	0.95	THERMAL SENSOR		
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	9 OF 43	

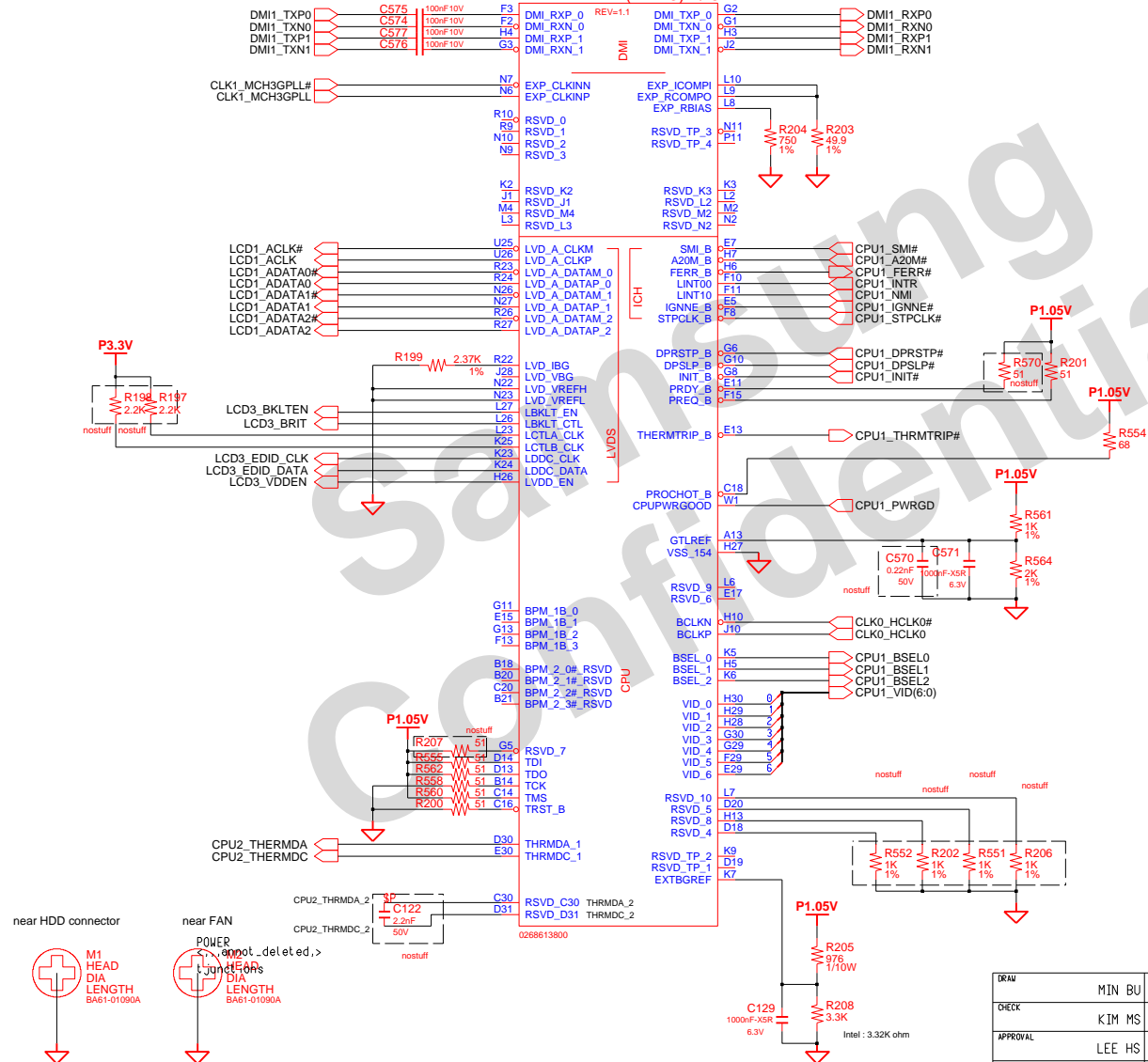
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PINEVIEW(1/3)

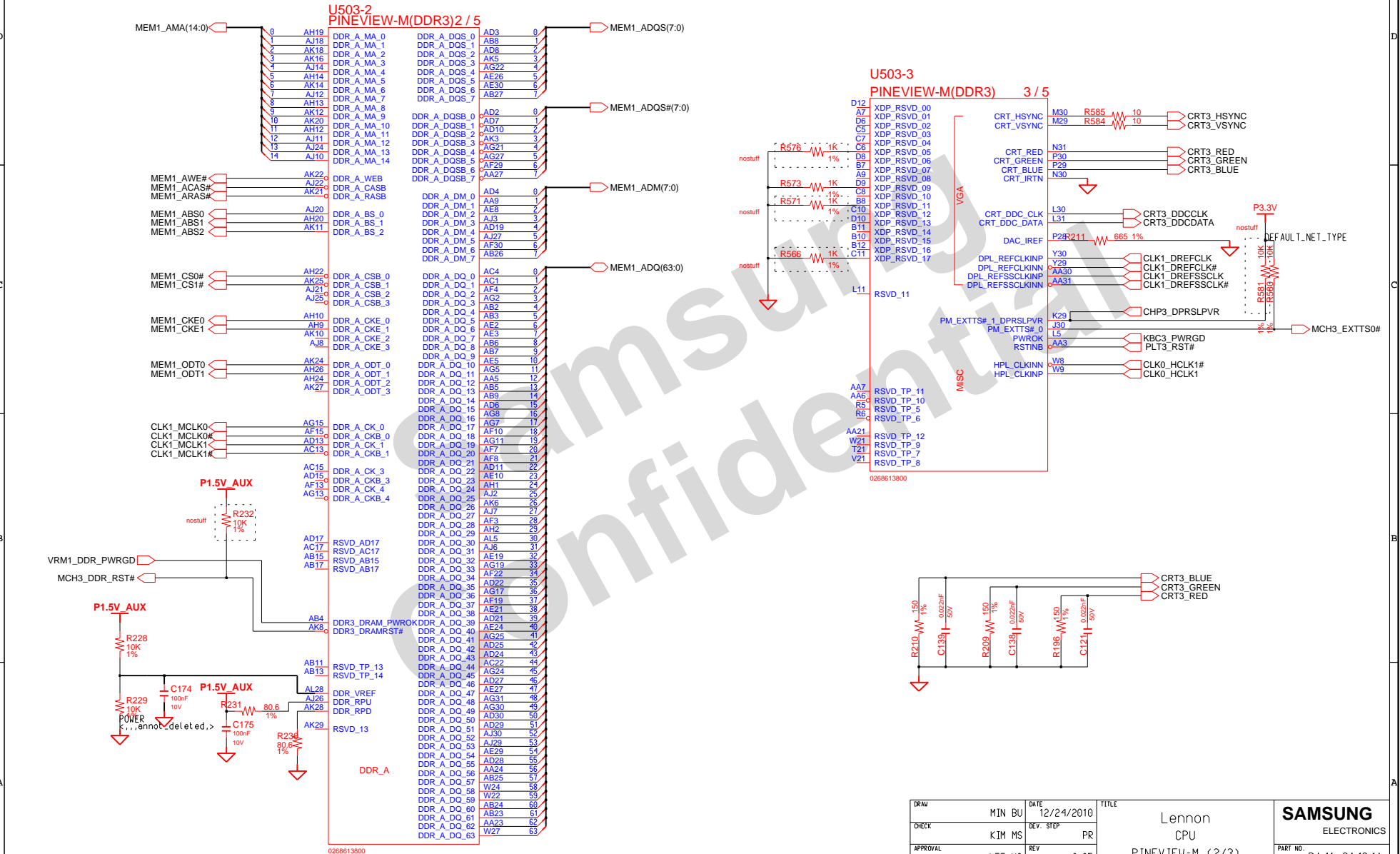
U503-1

PINEVIEW-M(DDR3)1 / 5



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CHECK	KIM MS	DEV. STEP	PR			PART NO. BA41-01494A
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	10	OF 43

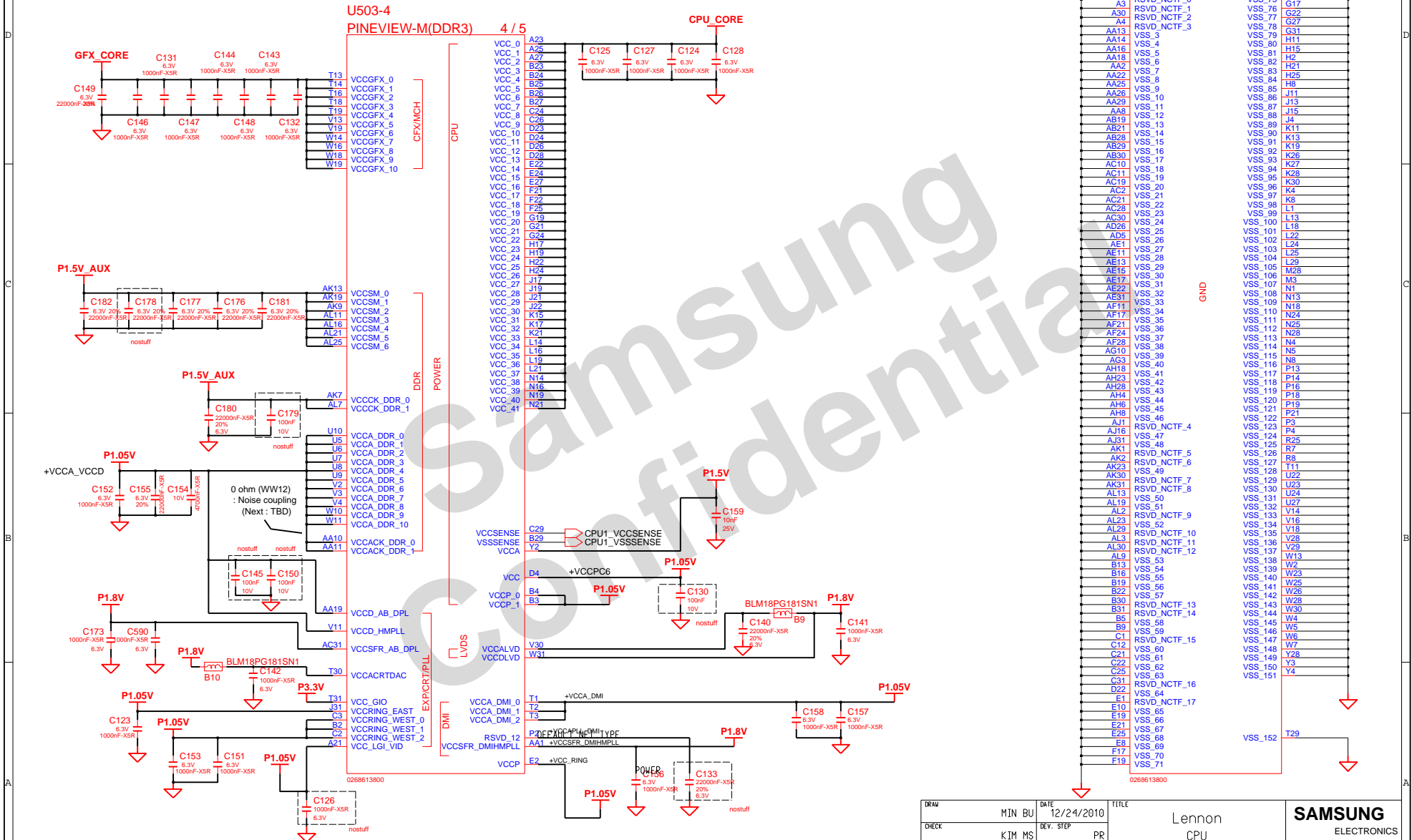
PINEVIEW(2/3)



DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon CPU	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			
APPROVAL	LEE HS	REV	0.95	PINEVIEW-M (2/3)	PART NO.	BA41-01494A
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	11	OF 43

PINEVIEW(3/3)

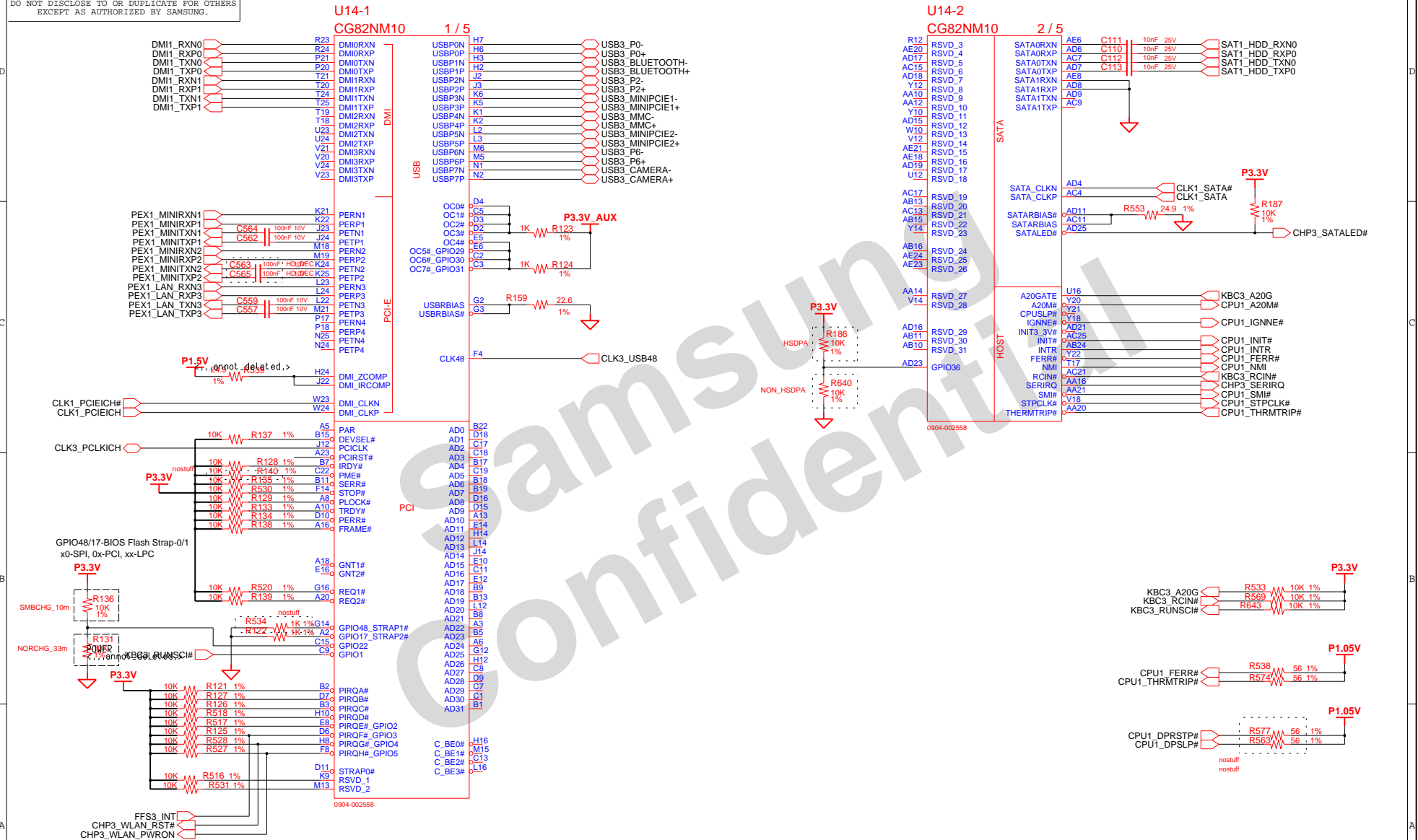
U503-5
PINEVIEW-M(DDR3)5 / 5



DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon CPU PINEVIEW-M (3/3)	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			
APPROVAL	LEE HS	REV	0.95			
MODULE CODE	LAST EDIT					
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					PART NO.	BA41-01494A
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Tigerpoint (1/3)



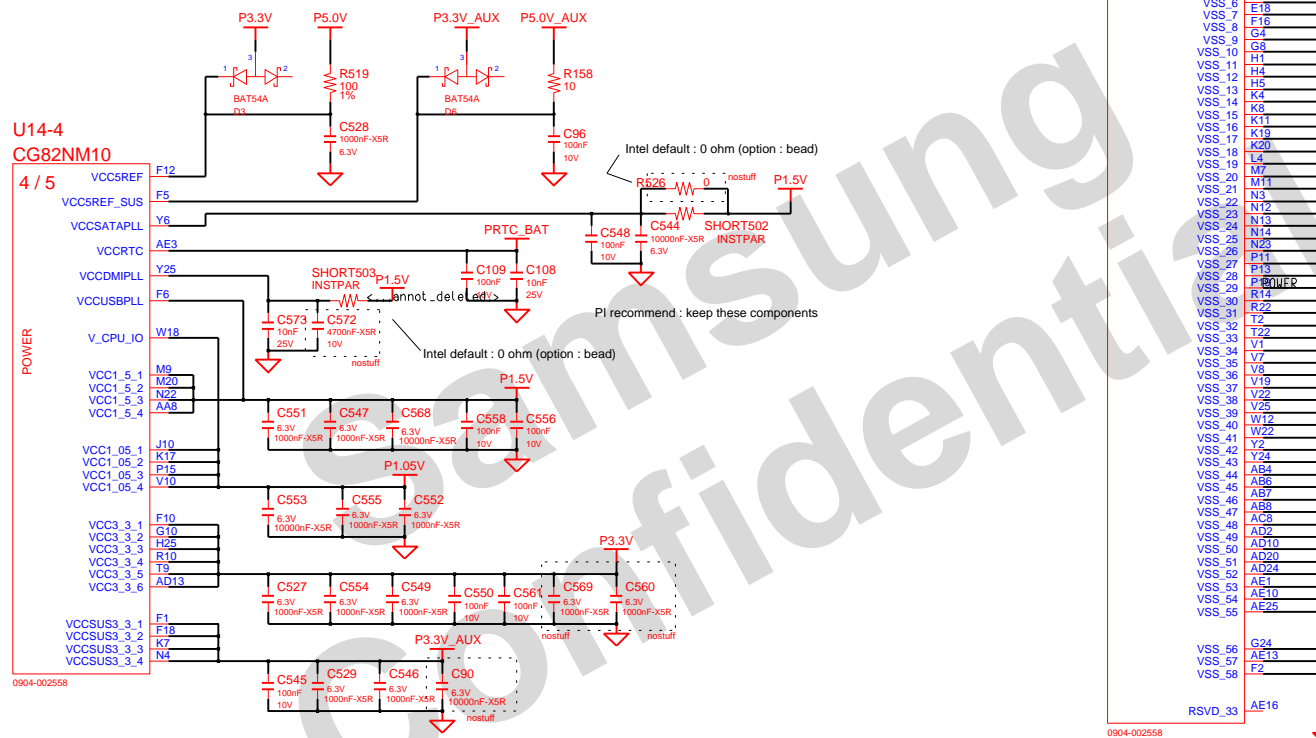
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CHECK	KIM MS	DEV. STEP	PR	CHIPSET		
APPROVAL	LEE HS	REV	0.95	TIGERPOINT (1/3)	PART NO.	
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM		BA41-01494A	

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U14-5
CG82NM10



DRAW	MIN BU	DATE	12/24/2010	TITLE Lennon CHIPSET TIGERPOINT (3/3)	
CHECK	KIM MS	DEV. STEP	PR		
APPROVAL	LEE HS	REV	0.95		
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02	VERIFY REAL MODE	56	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	64	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	65	DISPLAY SHADOW MESSAGE
05	INIT. SYSTEM HW	66	DISPLAY NON-DISAPABLE SEGMENT
06	INIT. SHIPSET REG.	67	DISPLAY ERROR MESSAGE
08	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG.	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT A20 LINE TO POST	7E	GETTER SECTORWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7F	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGEMENT	82	DETECT AND INSTALL EXT. RS232C
11	INIT. TEND	84	TEST FOR TAIL REGISTER PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	9A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	9C	INIT. F2 PROMPT
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT.	9C	SETUP POWER MANAGEMENT
1A	8237 DATA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	INIT. INTERRUPT CONTROLLER	0F	TEST
20	TEST DRAM REFRESH	A4	INIT. TYEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	INIT. A20	AC	INIT. A20
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
30	COMPUTE THE CPU SPEED	80	CHECK FOR ERRORS
32	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
34	SHADOW CYCLE BIOS ROM	B4	TEST
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	TEST SCREEN
44	INIT. BIOS INTERRUPT	0E	TEST BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	UNKNOWN HANDLER ERROR
49	INIT. I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
4B	INIT. VIDEO BIOS CONFIGURE AGAINST CMOS	D4	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
4E	PLAY COPYRIGHT PE AND SPEED	DC	SHUTDOWN 10
50	TEST KEYBOARD	89	ENABLE NMI
54	SET KEY/LCK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR EXPECTED INTERRUPTS	92	INIT. LOCAL BUS HDD CONTROLLER
5A	DISABLE POST SETUP	94	DISABLE LOCAL ADDRESS LINE
5C	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PART 1		

Diagram illustrating the pin connections for the J521 HDR-10P-1R-SMD STP component. The component is connected to the LPC3114 signals as follows:

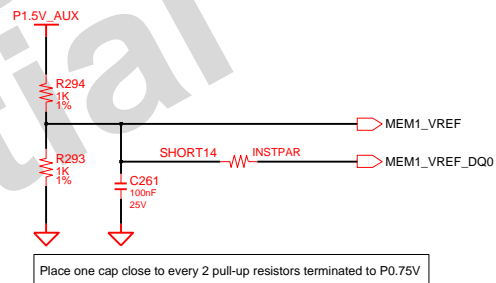
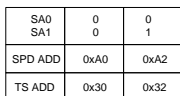
- Pin 1: PLT3_RST#
- Pin 2: CLK3_DBG/LPC
- Pin 3: LPC3_LFRAME#
- Pin 4: LPC3_LAD(3)
- Pin 5: LPC3_LAD(2)
- Pin 6: LPC3_LAD(1)
- Pin 7: LPC3_LAD(0)
- Pin 8: LPC3_LAD(0)
- Pin 9: LPC3_LAD(0)
- Pin 10: LPC3_LAD(0)
- Pin 11: MNT1
- Pin 12: MNT2

The component is labeled J521 HDR-10P-1R-SMD STP and is associated with the part number 3711-000386. A 3.3V supply is connected to pin 1, and a ground symbol is connected to pin 12.

DRAM	MIN BU	DATE	12/24/2010	TITLE	Lennon	
CHECK	KIM MS	DEV. STEP	PR	SPI_BIOS_ROM		
APPROVAL	LEE HS	REV	0.95	SPI_BIOS_ROM		
MODULE CODE	LAST EDIT		December 29, 2010 21:04:12 PM		PAGE 16 OF 43	

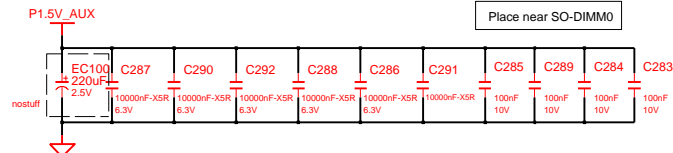
Height : 4 mm (STANDARD)

P/N : 3709-001607 (Concraft)



Place one cap close to every 2 pull-up resistors terminated to P0.75V

Place near SO-DIMM0

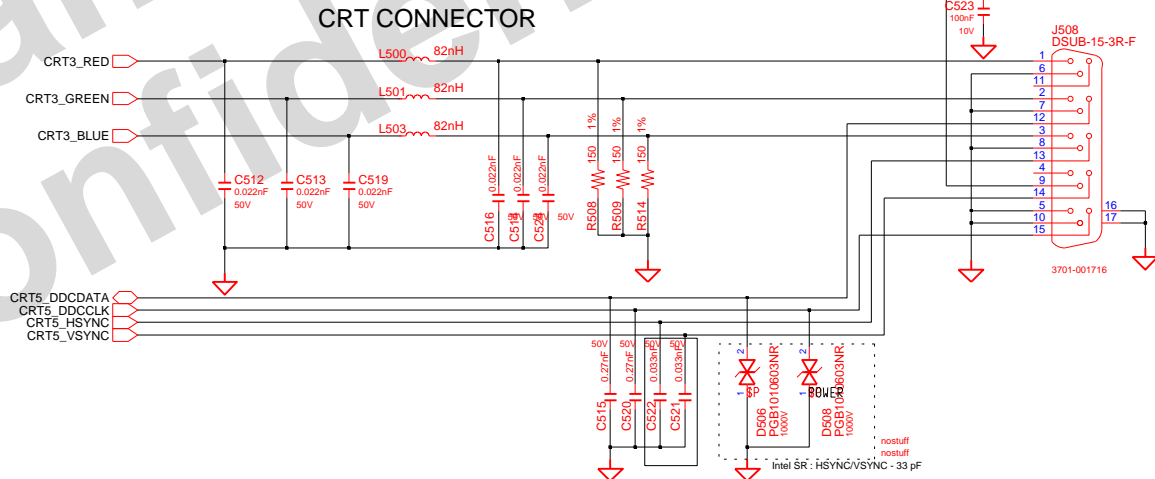
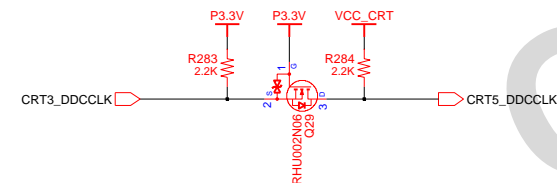
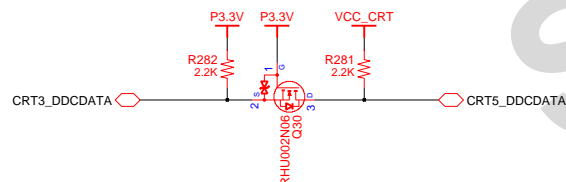
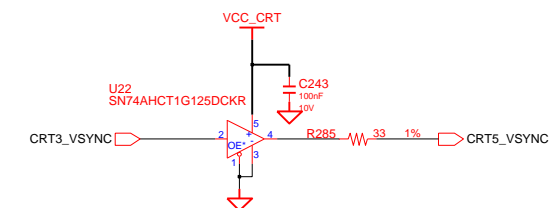
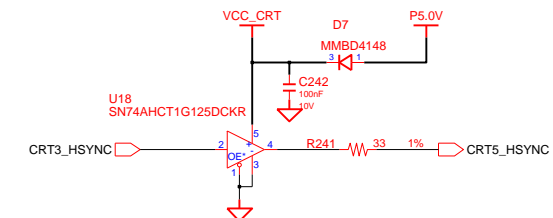


DRAM	MIN BU	DATE	12/24/2010	TITLE	Lennon SODIMM_DDR3 SODIMM_DDR3 #1	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			
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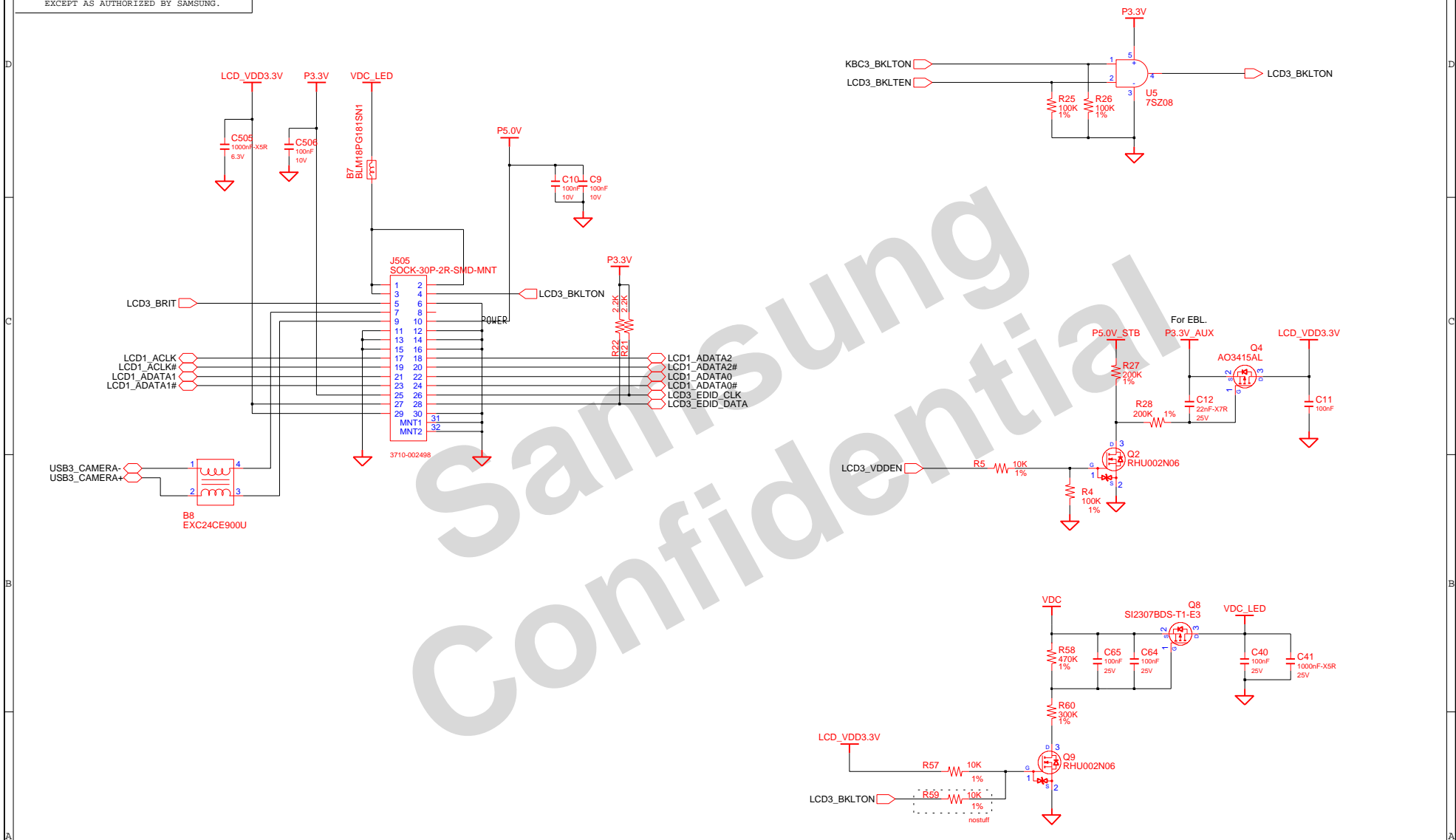
CRT



DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR	GRAPHICS_IF		
APPROVAL	LEE HS	REV	0.95	CRT		
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM			
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DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon GRAPHICS_IF LED LCD I/F	SAMSUNG ELECTRONICS PART NO. BA41-01494A
CHECK	KIM MS	DEV. STEP	PR			
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DRAW	MIN BU	DATE	12/24/2010	TITLE	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV.	STEP PR	Lennon Blank Page	
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MODULE CODE	undef ined	LAST EDIT	December 29, 2010 21:04:12 PM	PAGE 20 OF 43	

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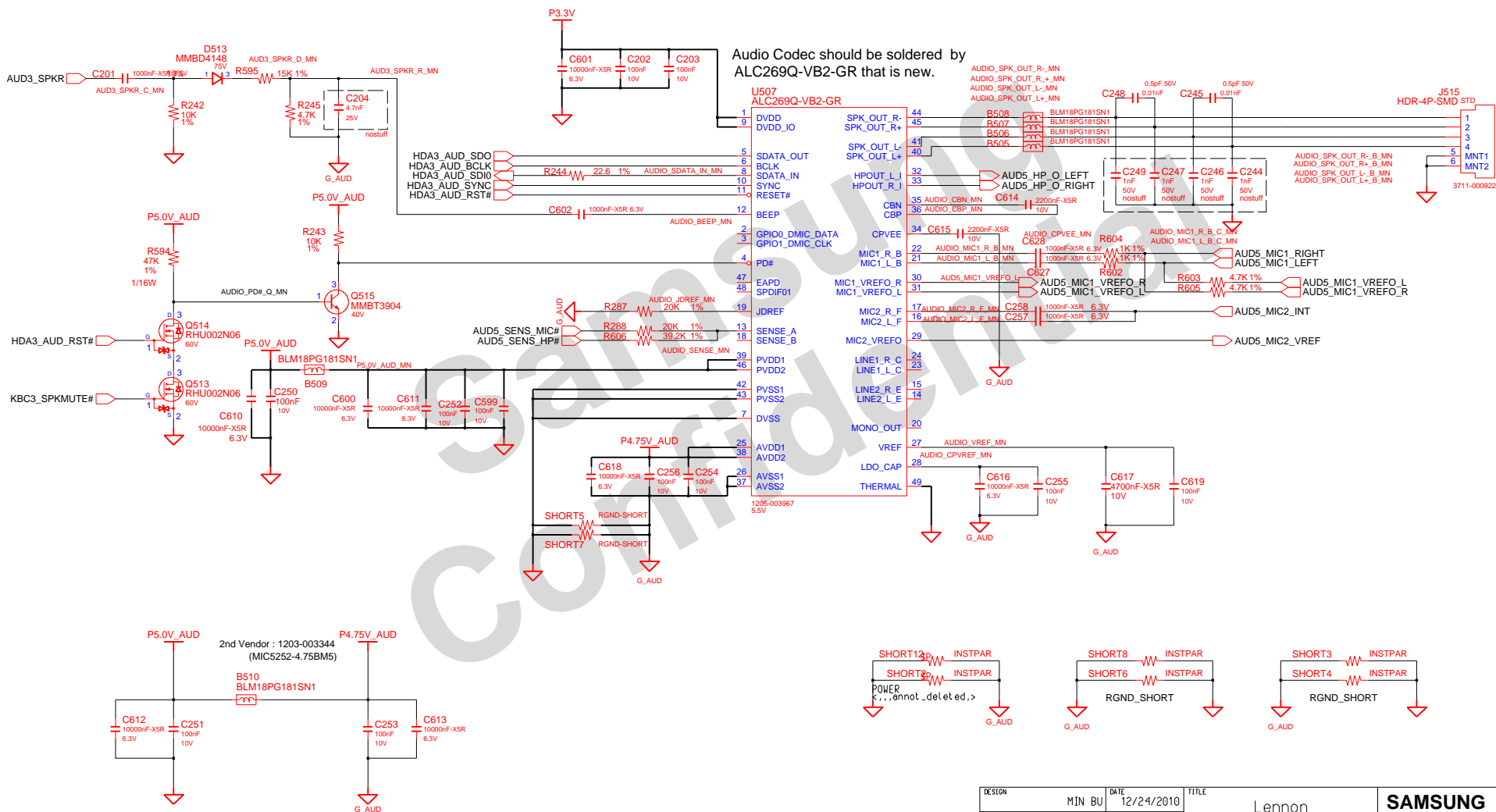
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CHECK	KIM MS	DEV. STEP	PR	Blank Page		
APPROVAL	LEE HS	REV	0.95	Blank Page	PART NO.	
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	21 OF 43	

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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

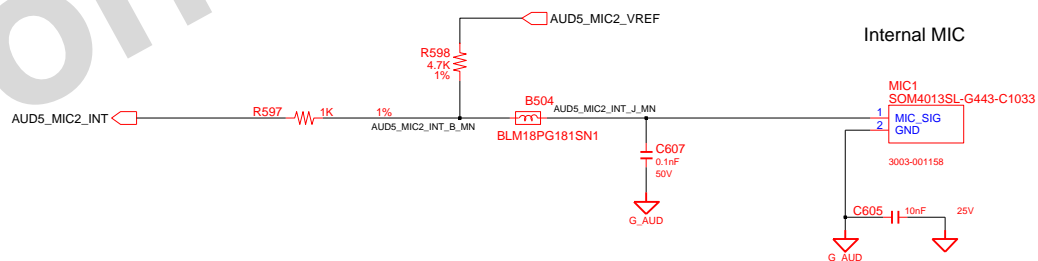
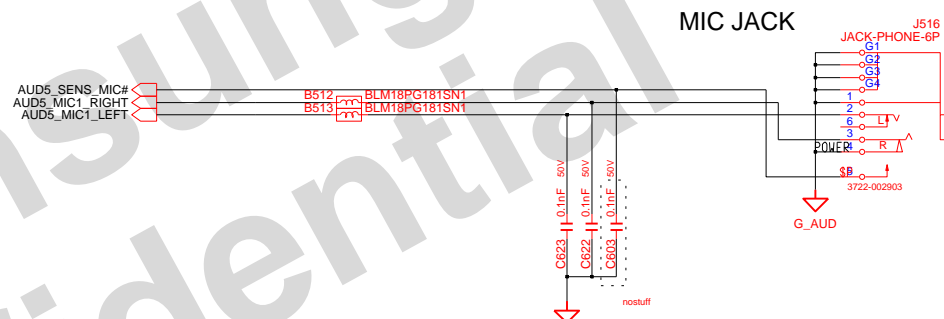
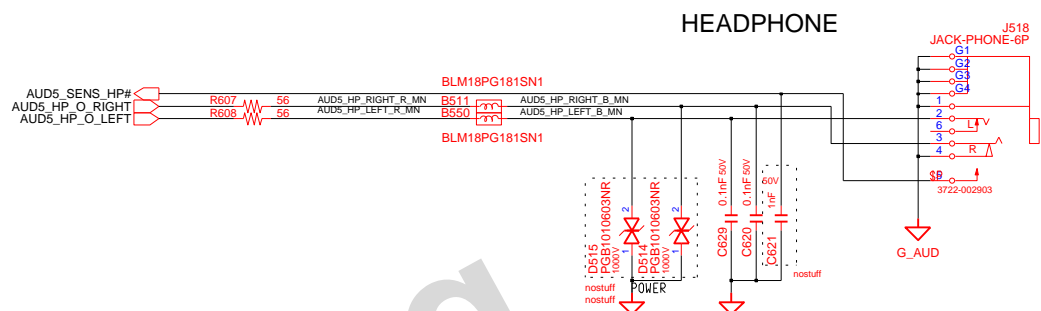
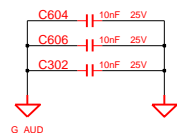
Audio Codec should be soldered by ALC269Q-VB2-GR that is new.



DESIGN	MIN BU	DATE	12/24/2010	Lennon AUDIO ALC269Q-VB	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR		
APPROVAL	LEE HS	REV	0.95		
MODULE CODE		LAST EDIT			
				December 29, 2010 21:04:12 PM	PAGE 22 OF 43

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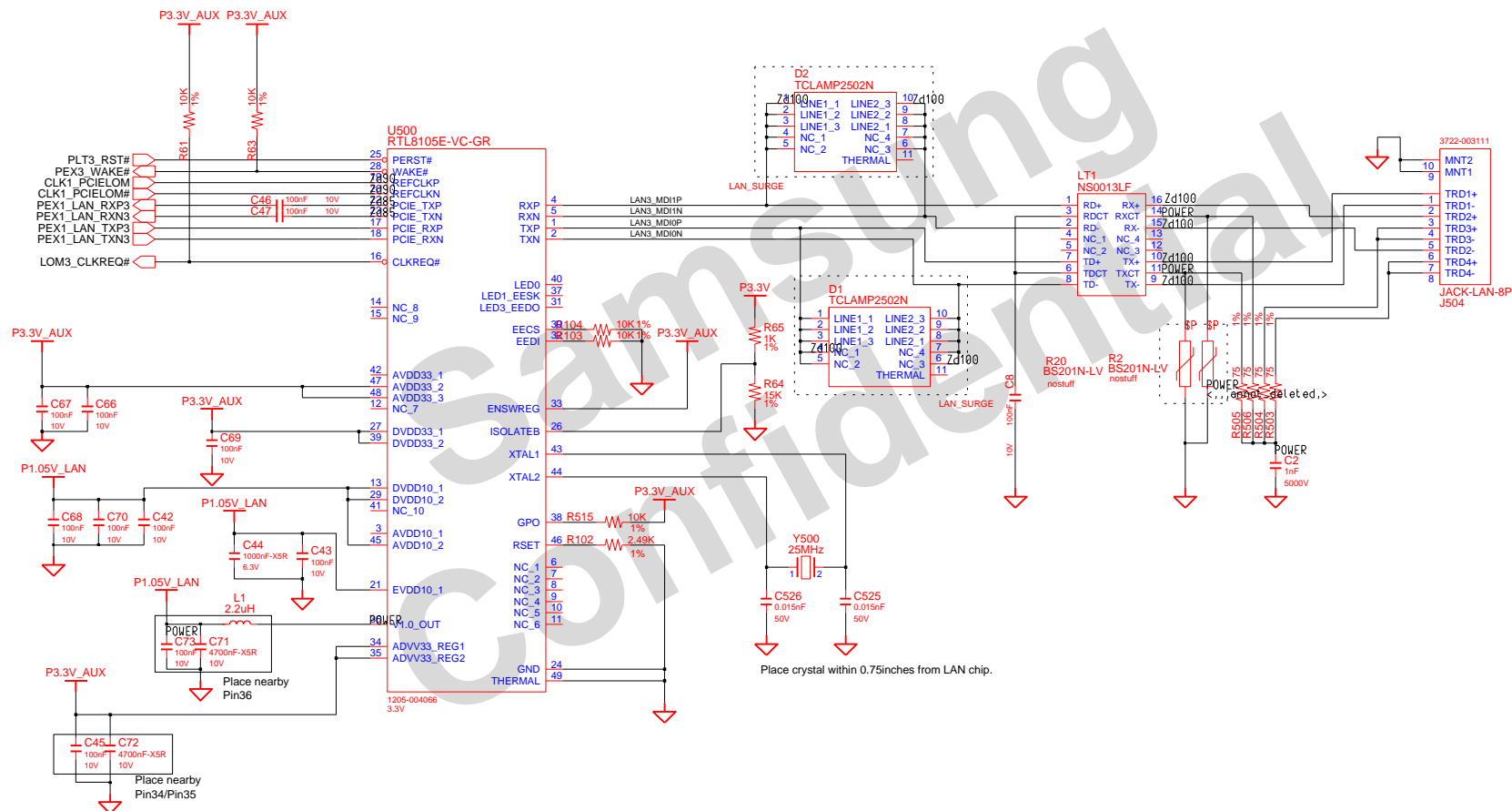


DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon AUDIO AUDIO	SAMSUNG ELECTRONICS PART NO. BA41-01494A
CHECK	KIM MS	DEV. STEP	PR			
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	23 OF 43	

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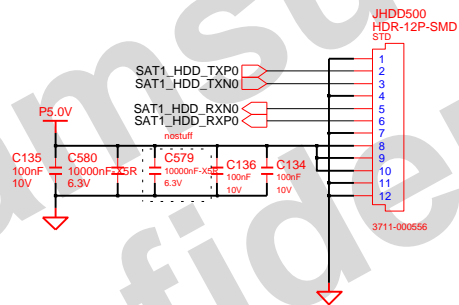
Realtek RTL8105E



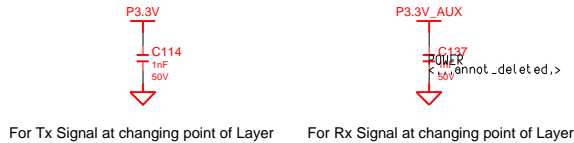
DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon LAN RTL8105E	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			PART NO. BA41-01494A
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	24	OF 43

SATA I/F CONN

SATA HDD CONN



For EMI



DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG
CHECK	KIM MS	DEV. STEP	PR	SATA_DEVICES		ELECTRONICS
APPROVAL	LEE HS	REV	0.95	SATA I/F	PART NO.	BA41-01494A
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	25	OF 43

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3709-001498

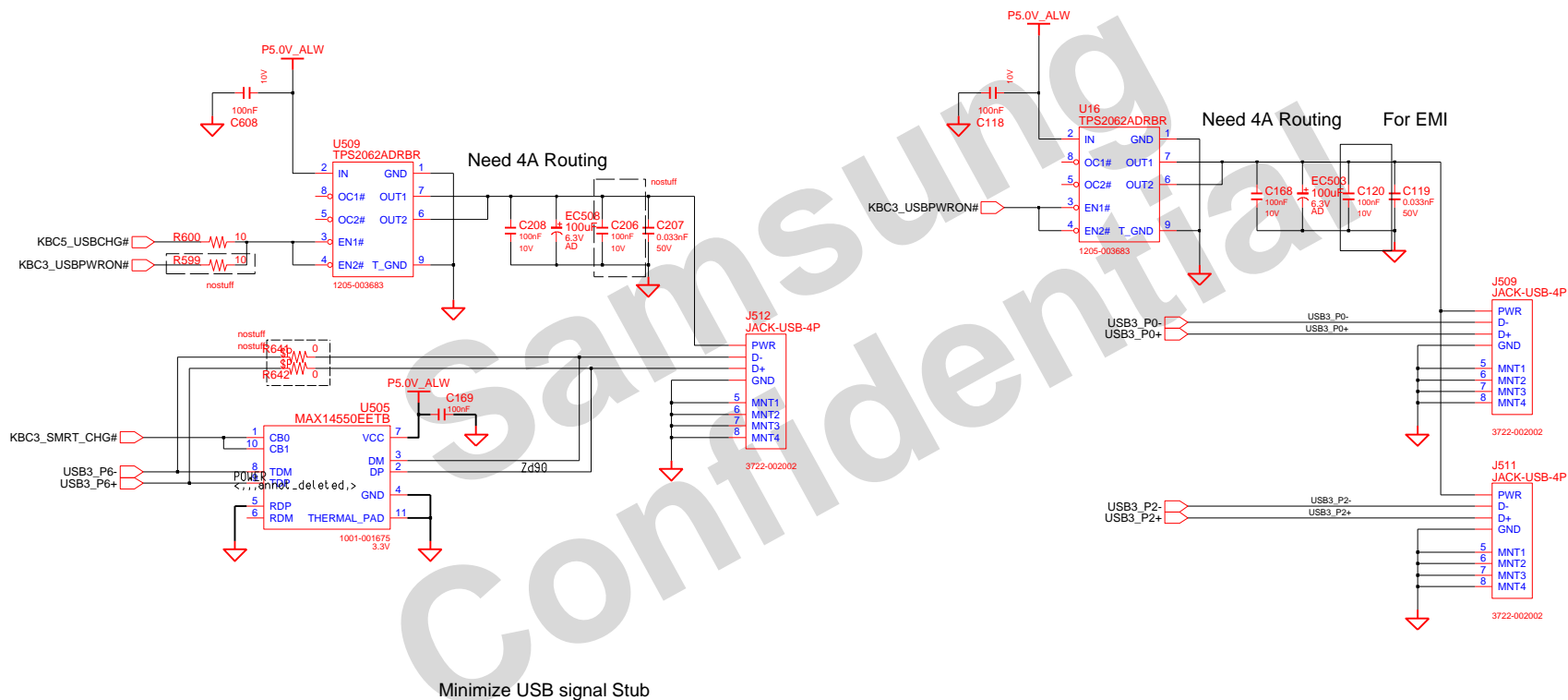
Near to Mini card Connector

PEM for Half length card
M500
HEAD
DIA
LENGTH
BA61-01090A

Mini-PCI Express Card
30.00 mm
48.00 mm
50.95 mm
Pin 1
Odd Pins : Top side
Even Pins : Bottom Side

DESIGN	MIN BU	DATE	12/24/2010	Lennon MINI_PCIE_CONN MINI PCI	SAMSUNG ELECTRONICS		
CHECK	KIM MS	DEV. STEP	PR				
APPROVAL	LEE HS	REV	0.95				
MODULE CODE	LAST EDIT		December 29, 2010 21:04:12 PM			PAGE	26
				PART NO.	BA41-01494A		

2 PORT USB CONNECTOR

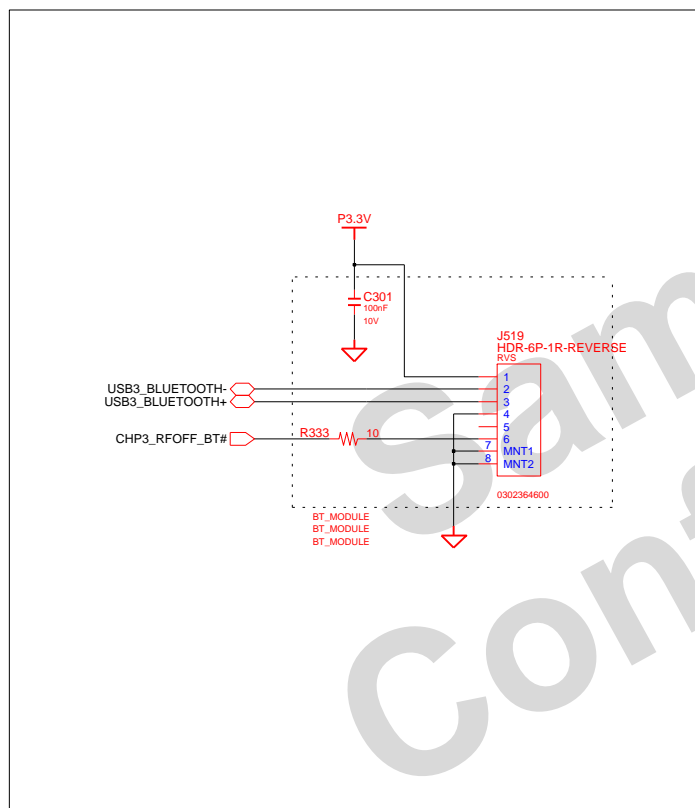


DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon USB_CONN USB PORT	
CHECK	KIM MS	DEV. STEP	PR			
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT		December 29, 2010 21:04:12 PM	PAGE	27 OF 43

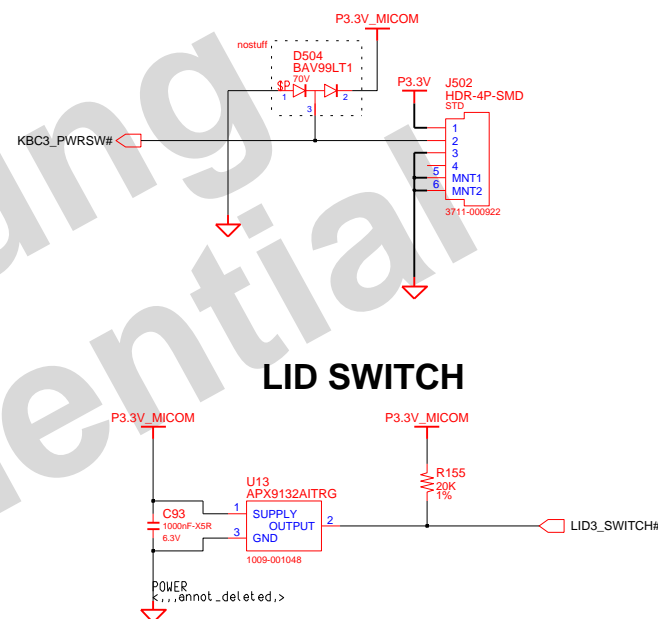
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Bluetooth Interface

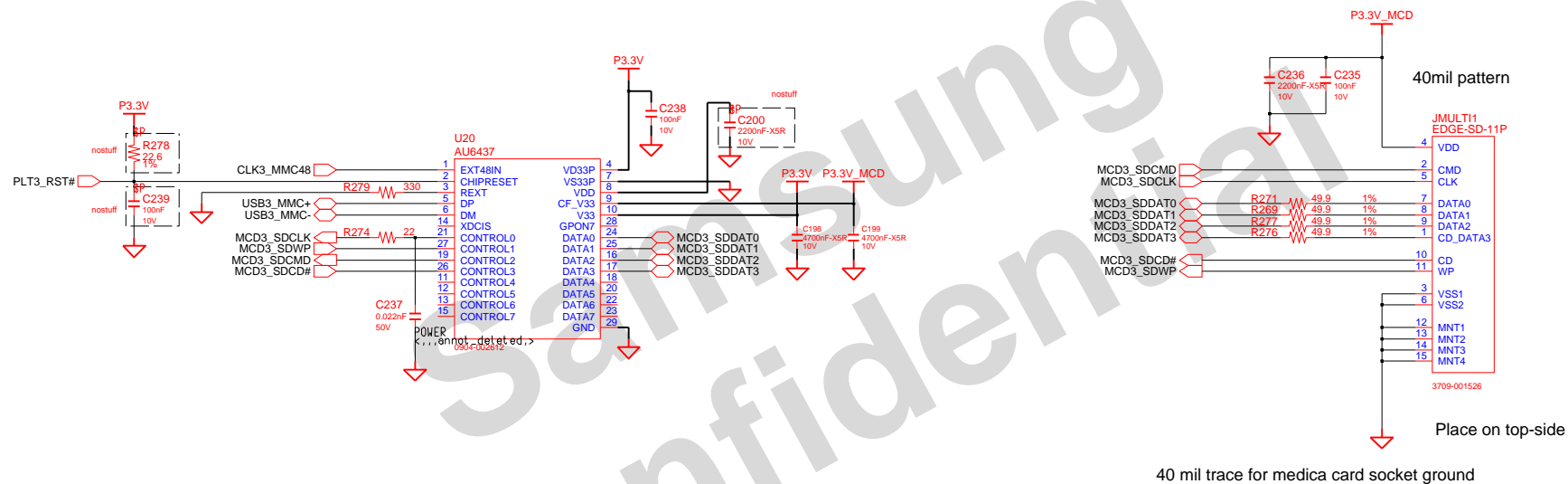



Power Switch Board Connector



DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR	USB_DEVICES SB I/F		
APPROVAL	LEE HS	REV	0.95	BLUETOOTH, System B'D I/F	PART NO. BA41-01494A	
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	28 OF 43	

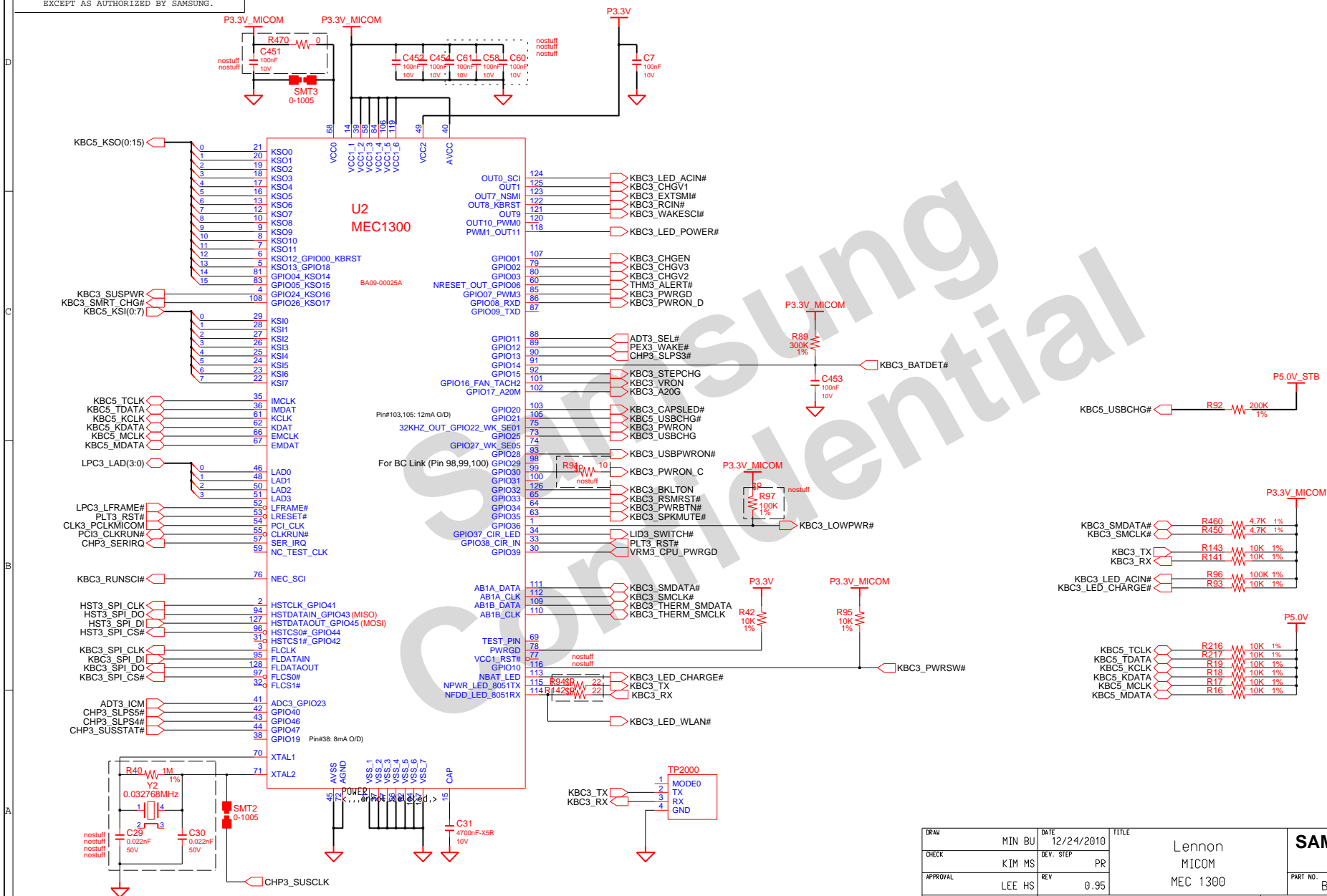
MMC(AU6437)



DATE	12/24/2010	TITLE	Lennon		
MIN BU		DEV. STEP	MMC		
CHECK	KIM MS	PR	AUG437		
APPROVAL	LEE HS	REV	0.95		
MODULE CODE		LAST EDIT		December 29, 2010 21:04:12 PM	PAGE 29 OF 43

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MAIN BOARD (MICOM) - SMSC MEC1300



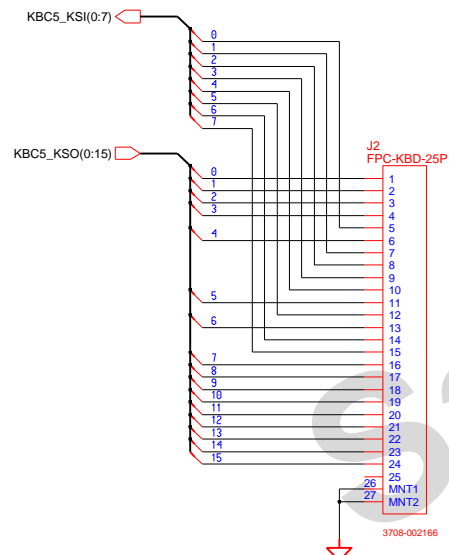
DRAM	MIN BU	DATE	12/24/2010	TITLE	Lennon MICOM MEC 1300	SAMSUNG ELECTRONICS		
CHECK	KIM MS	DEV. STEP	PR					
APPROVAL	LEE HS	REV	0.95					
MODULE CODE	LAST EDIT		December 29, 2010 21:04:12 PM				PAGE	30
						PART NO.	BA41-01494A	

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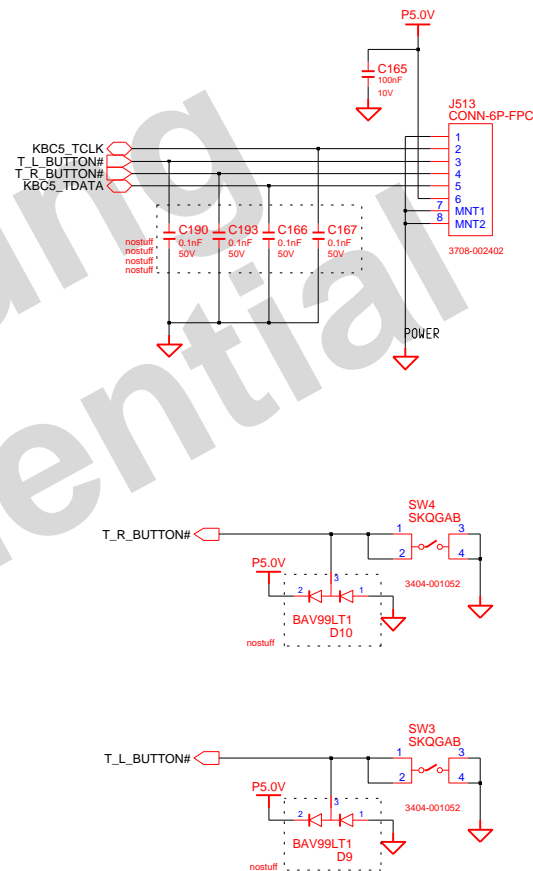
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Micom Glue Logic

KEYBOARD

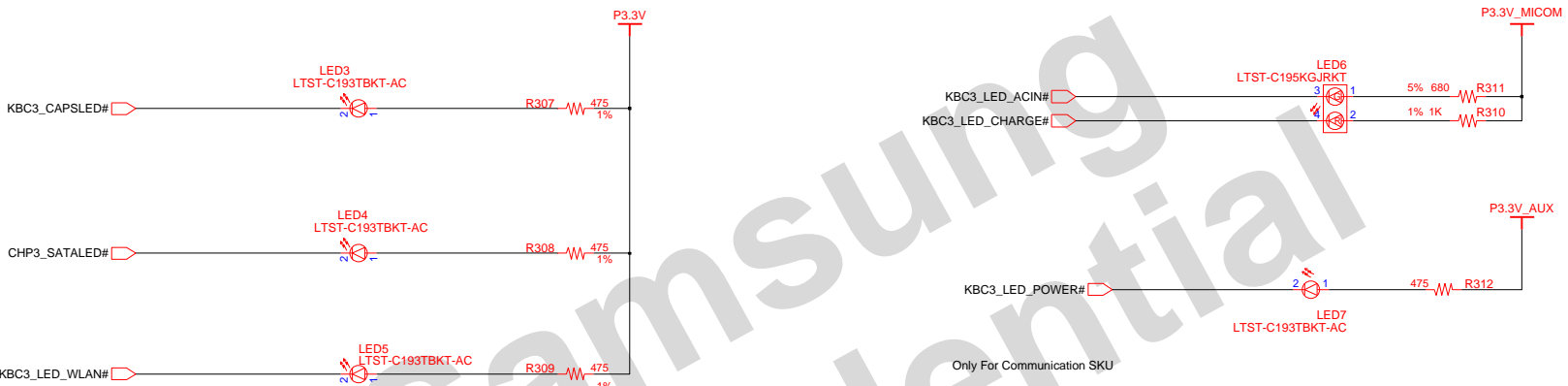


TOUCHPAD



DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon MICOM MICOM GLUE LOGIC	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			PART NO. BA41-01494A
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	31	OF 43

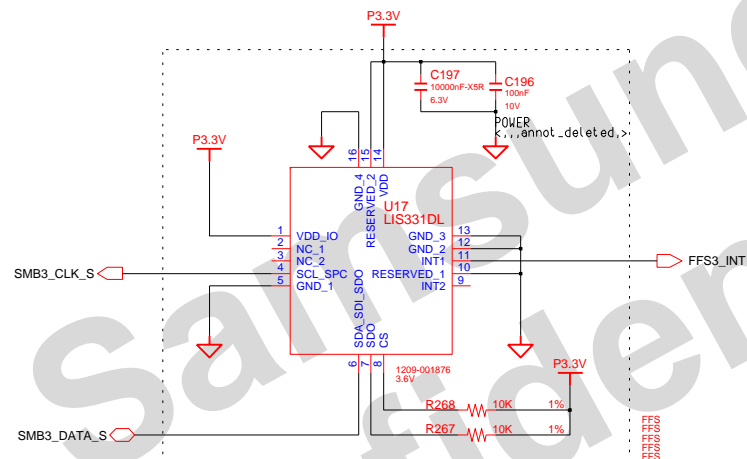
LED SWITCH LOGIC



DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			PART NO. BA41-01494A
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	32	OF 43

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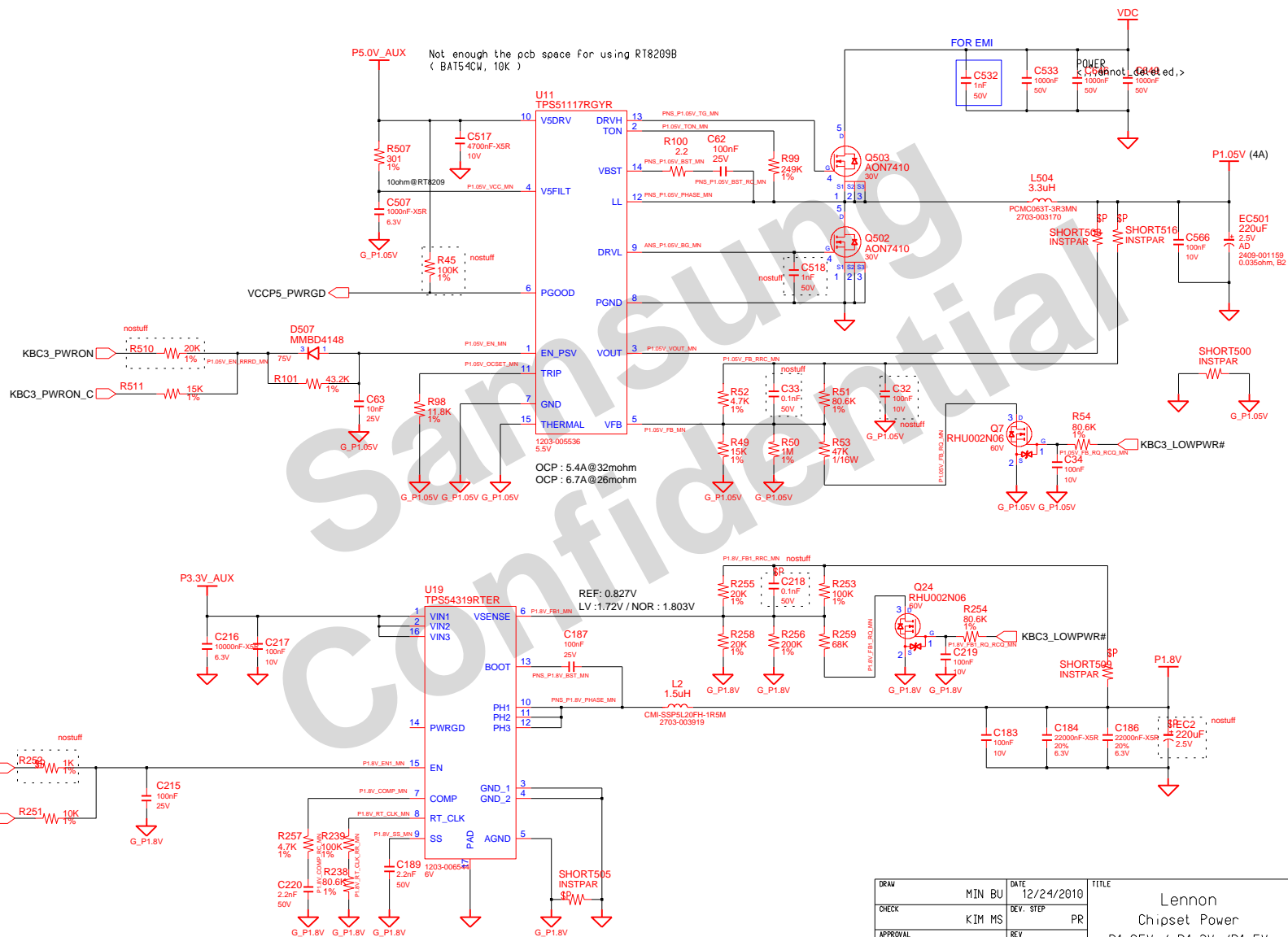
FREE FALL SENSOR

DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon FFS FreeFallSensor	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			PART NO. BA41-01494A
APPROVAL	LEE HS	REV	0.95			
MODULE CODE	undefined	LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	33	OF 43

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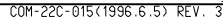
COM-22C-015(1996.6.5) REV. 3

Chipset Power (P1.8V & P1.05V)



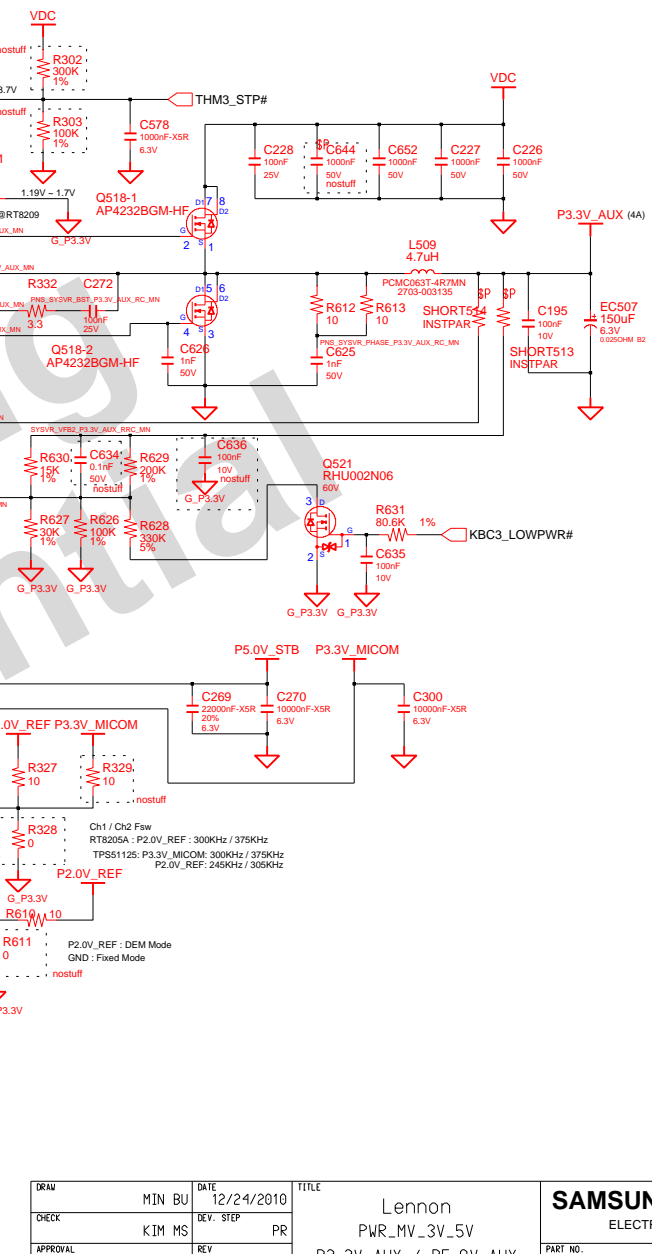
DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR	Chipset Power		
APPROVAL	LEE HS	REV	0.95	P1.05V / P1.2V / P1.5V	PART NO.	
MODULE CODE	undef ined	LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	35 OF 43	

COM-22C-015(1996.6.5) REV. 3

D:/users/mobile/mentor/lennon/1229_G0/Lennon_MAIN

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VDC



DRAW	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG	
CHECK	KIM MS	DEV. STEP	PR		PWR_MV_3V_5V	ELECTRONICS	
APPROVAL	LEE HS	REV	0.95		P3.3V_AUX / P5.0V_AUX	PART NO.	BA11-01494A
MODULE CODE	undefined	LAST EDIT	December 29, 2010 21:04:12 PM			PAGE	37 OF 43

CHARGER & POWER MANAGEMENT

[illegible]

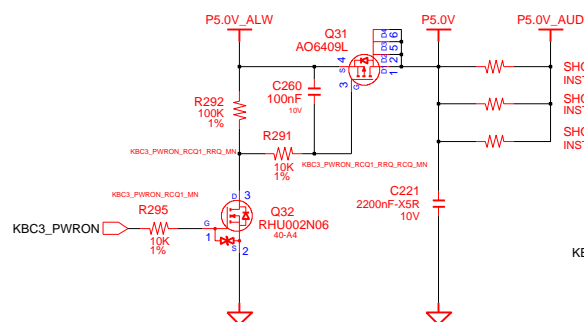
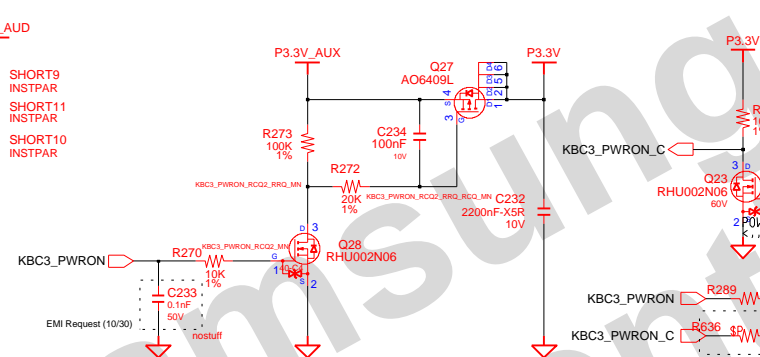
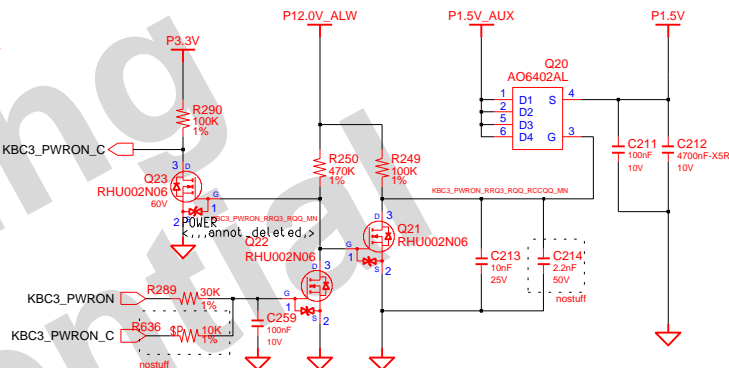
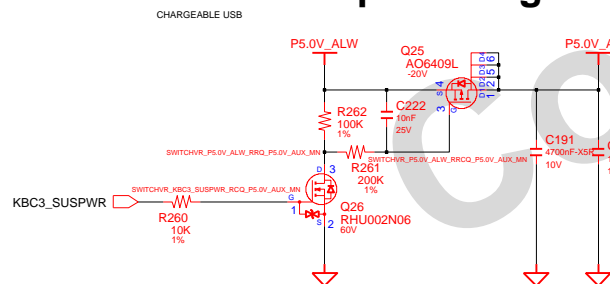
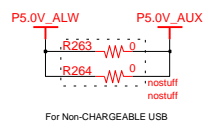
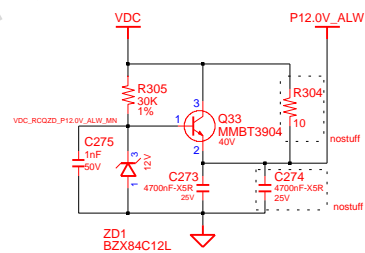
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[illegible]

COM-22C-015(1996.6.5) REV. 3


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Load Switch Control (P5.0V)**Load Switch Control (P3.3V)****Load Switch Control (P1.5V)****Sleep'n Charger****P12V_ALW**

DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon Switched PWR Switched PWR	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR			PART NO. BA41-01494A
APPROVAL	LEE HS	REV	0.95			
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	40	OF 43

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DRAM	MIN BU	DATE	12/24/2010	TITLE Lennon Discharger Discharger	
CHECK	KIM MS	DEV. STEP	PR		
APPROVAL	LEE HS	REV	0.95		
MODULE CODE		LAST EDIT			
				December 29, 2010 21:04:12 PM	PAGE 41 OF 43

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Blank Page

DESIGN	MIN BU	DATE	12/24/2010	TITLE	Lennon	SAMSUNG ELECTRONICS
CHECK	KIM MS	DEV. STEP	PR	Blank Page		
APPROVAL	LEE HS	REV	0.95	Power/SmartBrowsing	PART NO.	
MODULE CODE		LAST EDIT	December 29, 2010 21:04:12 PM	PAGE	42 OF 43	

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Top + Bottom
(Bottom side)

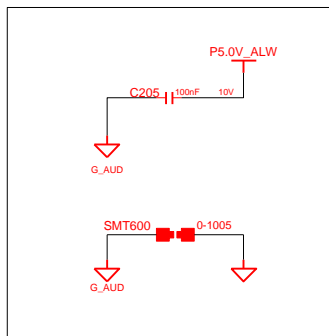
KBD

M/B
+
Top

M502
HEAD
DIA
LENGTH
BA61-01260A

M503
HEAD
DIA
LENGTH
BA61-01260A

M504
HEAD
DIA
LENGTH
BA61-01260A



FOR EMI

Dummy (LED side)

multi_assy selection

	BT_COMBO	BT_MODULE	HSDPA	LAN_SURGE	FFS
WLAN + BT Module	X	O	X	X	X
WLAN/BT Combo	O	X	X	X	X
WLAN Only	X	X	X	X	X
HSPA + WLAN/BT	O	X	O	X	X
HSPA + WLAN	X	X	O	X	X
For China	D/C	D/C	D/C	O	X

* D/C stands for "Don't Care"

DATE	12/24/2010	TITLE	Lennon ETC ETC		SAMSUNG ELECTRONICS		
MIN BU		DEV. STEP					PR
CHECK	KIM MS						
APPROVAL	LEE HS	REV	0.95	PART NO.		BA41-01494A	
MODULE CODE	LAST EDIT		December 29, 2010 21:04:12 PM		PAGE	43 OF 43	